Fig.1 (Prior Art)

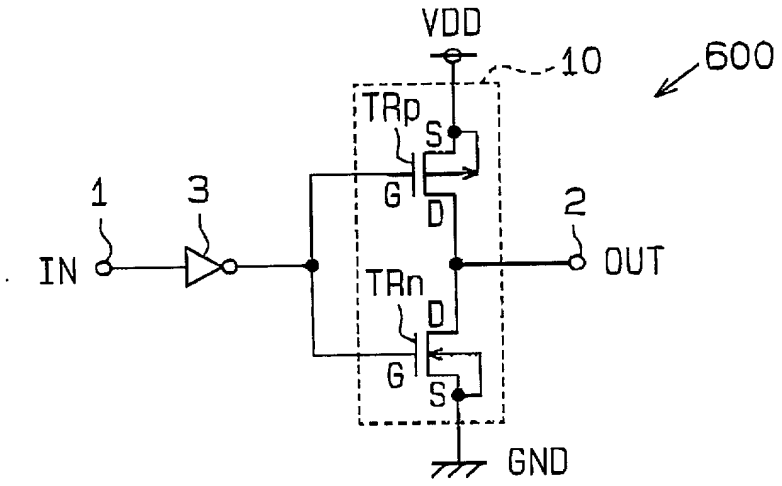


Fig.2

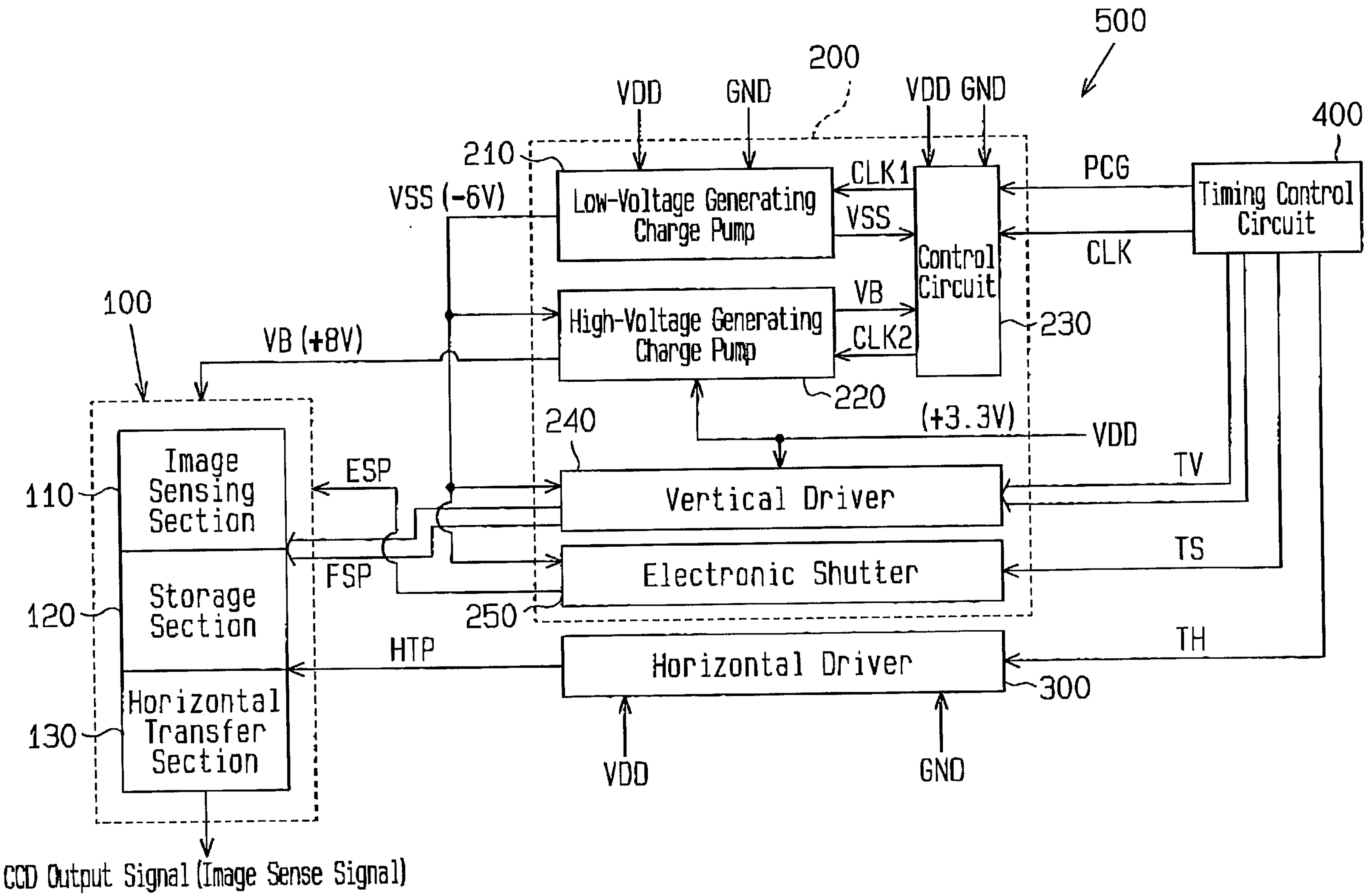
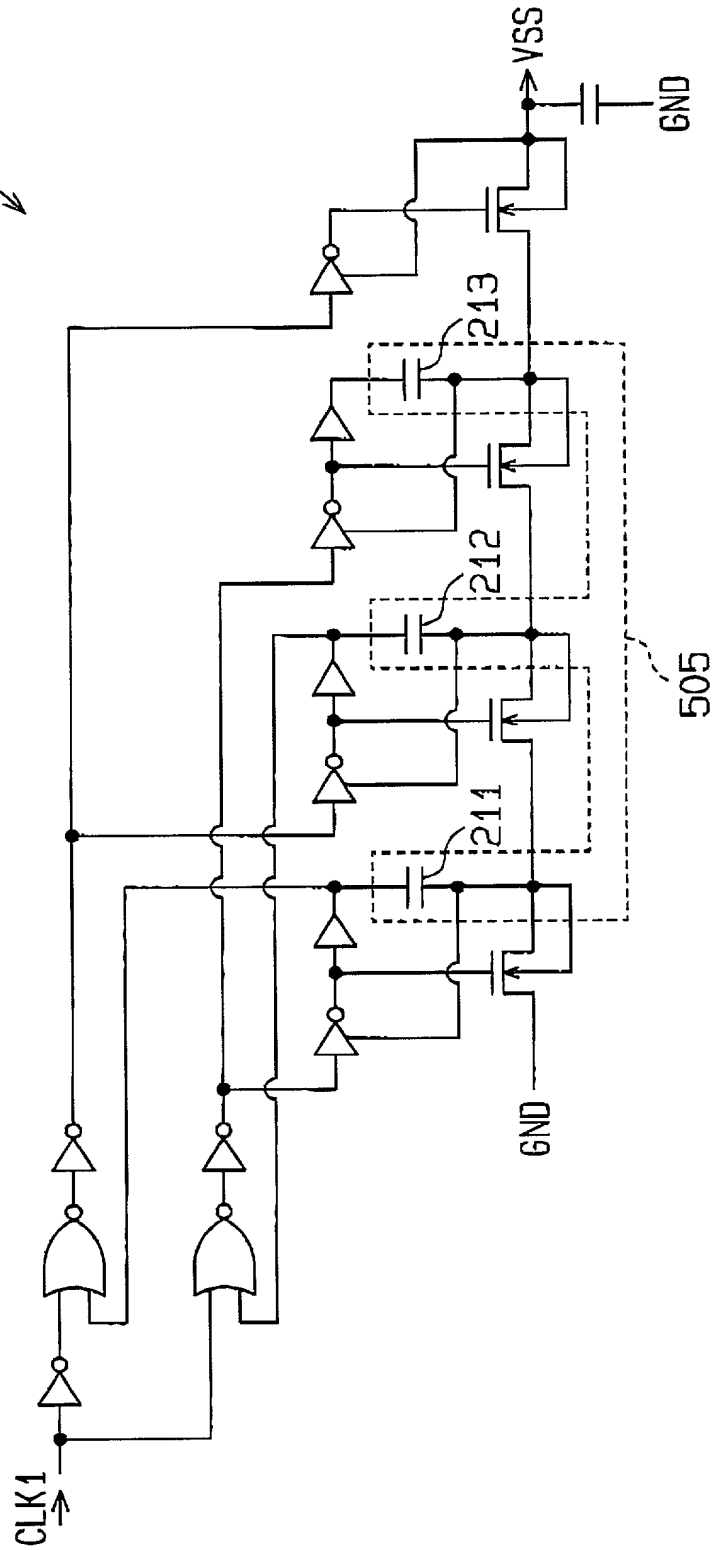

500
200
400
Timing Control Circuit
PCG
CLK
TV
TS
TH
VDD
GND
VDD GND
210
Low-Voltage Generating Charge Pump
High-Voltage Generating Charge Pump
220
Control Circuit
230
CLK1
VSS
VB
CLK2
(+3.3V)
VDD
VSS (-6V)
VB (+8V)
240
Vertical Driver
Electronic Shutter
250
Horizontal Driver
300
VDD
GND
ESP
FSP
HTP
100
Image Sensing Section
Storage Section
Horizontal Transfer Section
110
120
130
CCD Output Signal (Image Sense Signal)

Fig.3



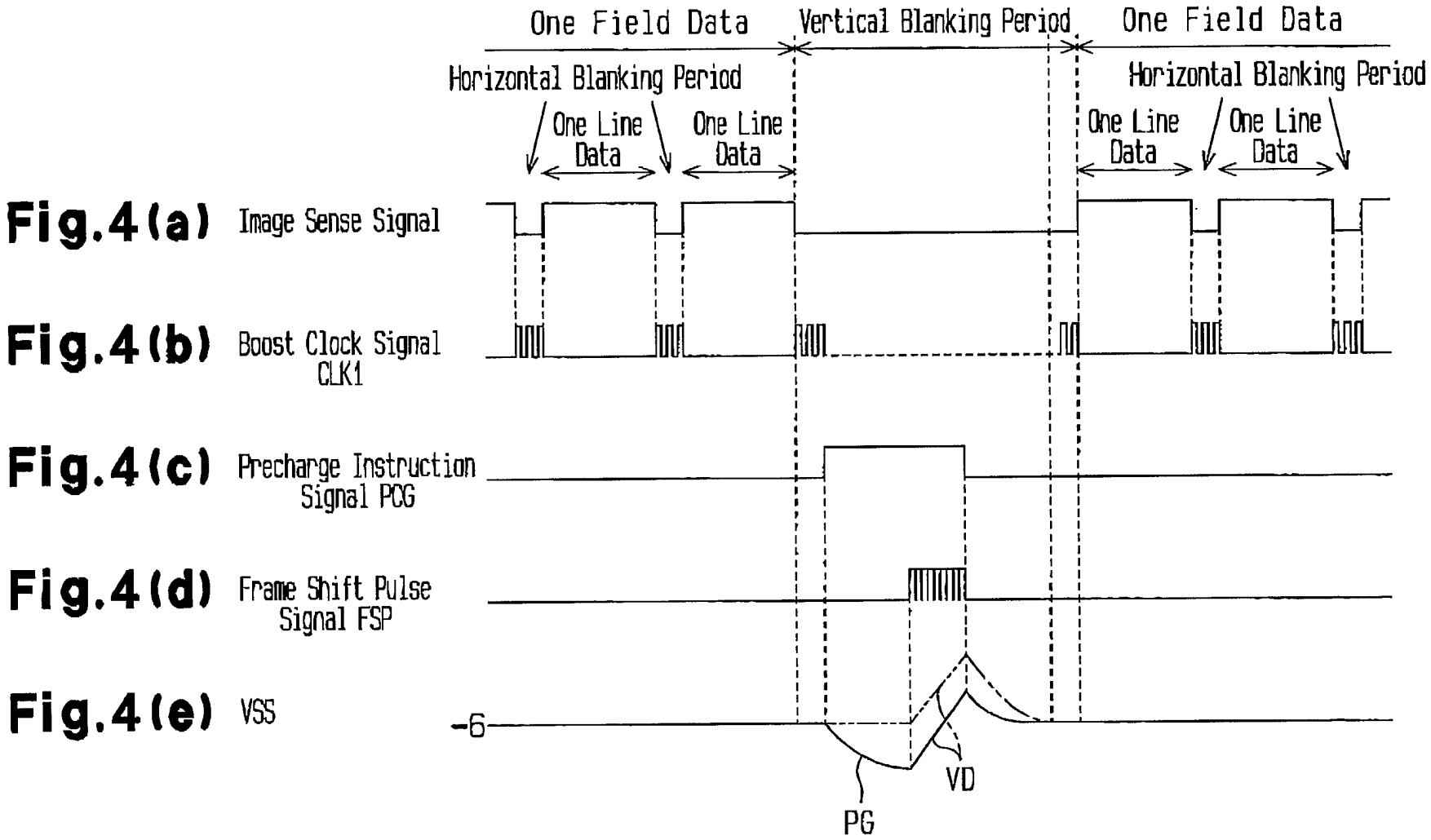


Fig.5

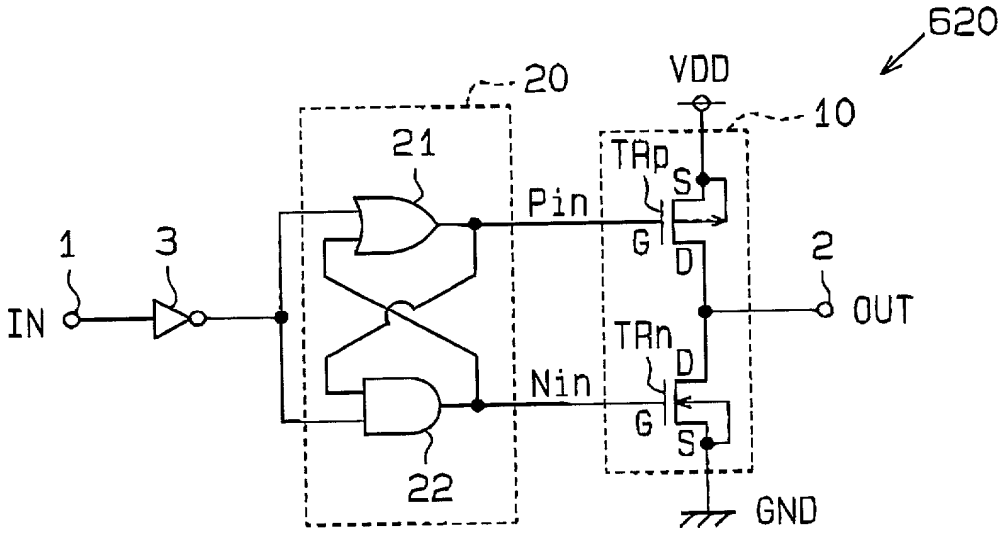


Fig.6(a) IN H (VDD) L (0)

Fig.6(b) Pin H L

Fig.6(c) Nin H L

Fig.6(d) OUT H L

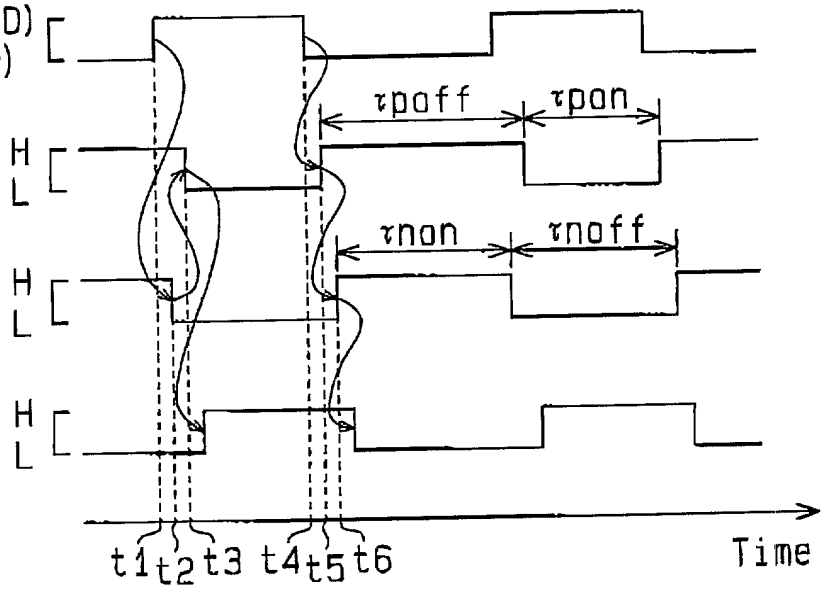


Fig.7

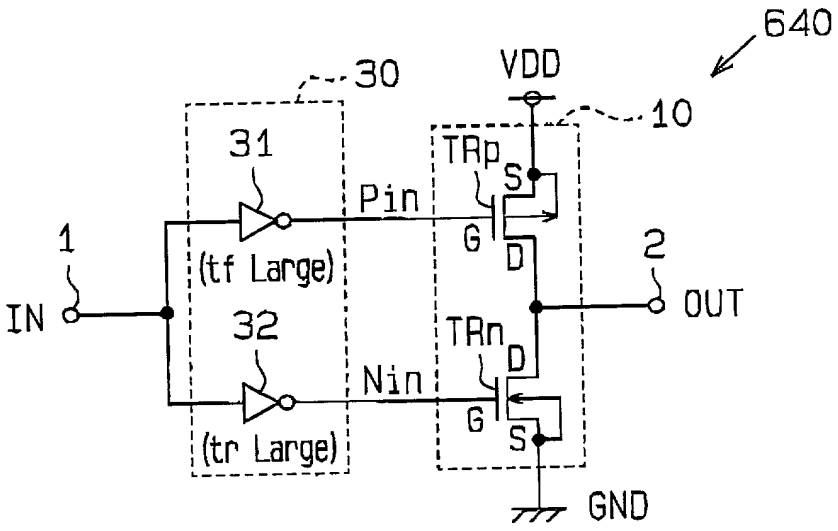


Fig.8(a) IN H (VDD) L (0)

Fig.8(b) Pin H L

Fig.8(c) Nin H L

Fig.8(d) OUT H L

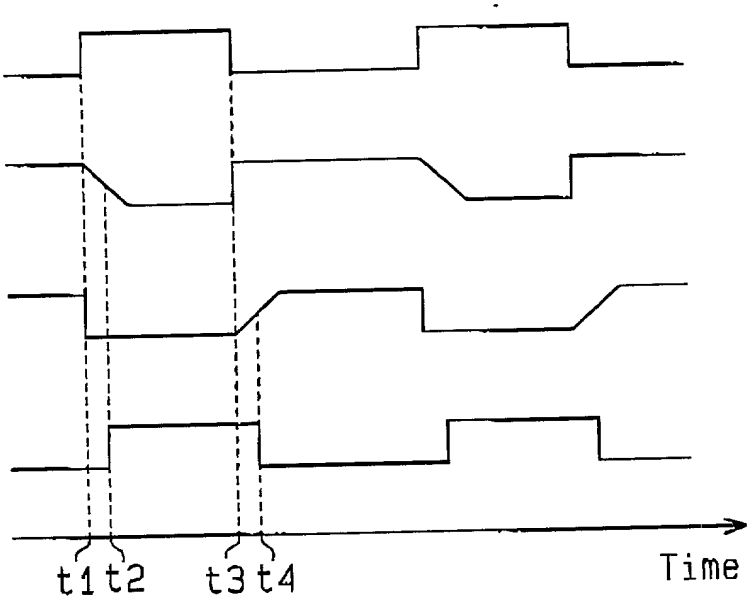


Fig.9

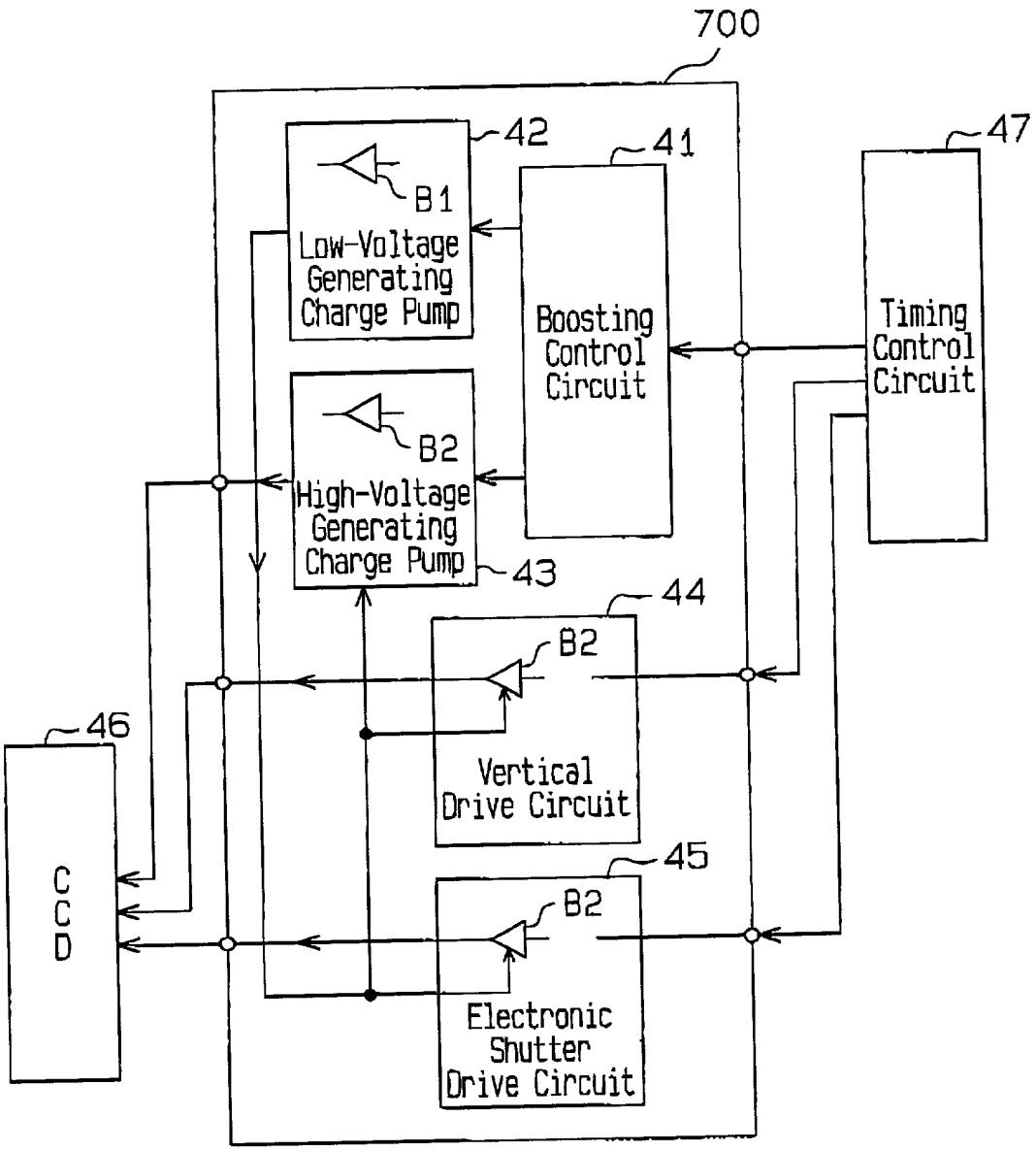
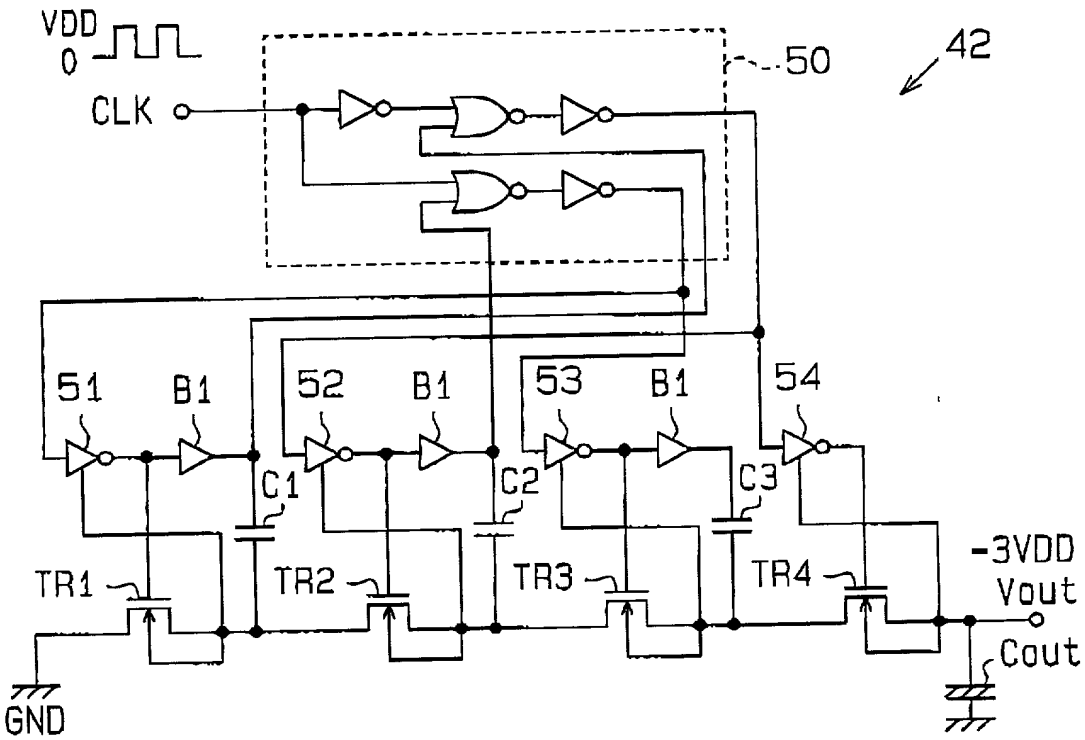

700
42
41
47
B1
Low-Voltage
Generating
Charge Pump
Boosting
Control
Circuit
Timing
Control
Circuit
B2
High-Voltage
Generating
Charge Pump
43
44
B2
Vertical
Drive Circuit
46
45
B2
CCD
Electronic
Shutter
Drive Circuit

Fig.10


VDD
0
CLK
50
42
51
B1
52
B1
53
B1
54
C1
C2
C3
TR1
TR2
TR3
TR4
-3VDD
Vout
Cout
GND